An aggregate dynamic model for distributed energy resources for power system stability studies

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Abstract:

As distributed generation penetration in power systems around the world continues to increase there is a pressing need for improved dynamic models for distributed energy resources for use in large scale power system simulation tools. This need has been heightened in the past few years in North America. Thus, the Renewable Energy Modeling Task Force of the Western Electricity Coordinating Council embarked on this task in late 2016, culminating with the development of a simple distributed energy resource model called DER A in 2018. This paper describes this model in detail and demonstrates the testing that was done to verify the implementation of the model in several commercial software tools.

1. Introduction

The focus on expansion of renewable resources is a continuing trend worldwide. Thus, wind and photovoltaic (PV) generation continue to be deployed within the power systems around the world at the transmission level. However, another rapidly growing sector is the deployment of distributed photovoltaic generation systems at the residential and commercial level. In the case of large utility scale wind and PV power plants, there has been much effort in recent years to develop simple, generic and publicly available dynamic models for simulating such technologies in commercially available power system simulation tools [1]. Also, with regards to wind generation, there is an International Electrotechnical Commission Working Group, nearing completion of an international

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KEYWORDS Distributed Energy Resource Modeling standard set of public models for wind turbine generators [2]. Also, CIGRE has recently published a Technical Brochure on the subject of inverter-based generation modeling [3].

With regards to the distributed energy resources (DER) there has not been a simple dynamic model that is available across multiple simulation platforms for use in large power system simulation studies. One model was developed many years ago called the PVD1 model [4]. This model, however, was not adopted by all commercial software vendors in North America and had some known limitations, from its inception, since at the time it was developed the proliferation of DER was still limited and the various standards related to DER were still under flux. With the recent approval of the revised IEEE Standard 1547 in April, 2018 [5], and other similar standards such as California Rule 21¹², more functionalities like voltage and frequency control are being proposed for DER. Hence, within the Western Electricity Coordinating Council's (WECC) Renewable Energy Modeling Task Force (REMTF), an effort was started to look at developing a new model for modeling DER, to be ultimately incorporated into the existing composite load model initially developed in WECC¹³. This paper outlines the development of this new model, gives a brief description of the model, and provides a summary of the testing of the model in several commercial power system simulation tools.

The remainder of this paper is organized as follows. In section 2, is a brief outline of the model and its salient features, as well as a description of how it is to be

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¹²⁻ http://www.cpuc.ca.gov/Rule21/

¹³⁻ https://www.wecc.biz/_layouts/15/WopiFrame.aspx?sourcedoc=/Reliability/WECC%20 Composite%20Load%20Model%20Specifications%2001-27-2015.docx&action=default&D efaultItemOpen=1



Figure 1: Location of DER plugging into the composite load model.

incorporated into the composite load model. In section 3, a description is given of a detailed testing that has been done of the model across four commercial software platforms. Also, in section 3, a brief description is given of running the model in large system studies, together with the composite load model, to compare it with *PVD1*. Finally, section 4 provides the conclusions and summary as well as some brief comments on future work.

2. The DER_A Model

The ultimate purpose of the distributed energy resource model version A (DER_A) is for it to be used to represent the aggregated dynamic behavior of the DER in timedomain positive-sequence stability studies. That is, this model would represent the combined (aggregated) dynamics behavior of many tens to hundreds of small distributed inverter-based generators on the distribution system on for example residential feeders – such as roof-top photovoltaic generation. As such, it will eventually be deployed as part of the composite load model, as shown in Figure 1.

The concept behind development of the *DER_A* model was to create a model that is able, to some extent, to emulate the key dynamic performance that may be required from such resources in the future, such as frequency and voltage control. At first sight the 2nd generation generic renewable energy source (RES) models [1], that were developed for inverter-based generation, may seem appropriate to use to model DER (i.e., *repc_a* + *reec_a* + *regc_a*). However, there are two drawbacks with this approach (i) they constitute well over one-hundred parameters and so are perhaps too complex for modeling aggregated DER, and (ii) the 2nd generation models were developed for modeling single large wind/PV and battery-energy storage plants and so may not provide a simple means to represent aggregated behavior across numerous distributed generators.

Thus, starting with the model structures of the 2nd generation RES models (i.e., repc a + reec a + regc a), a significantly reduced version of the core functionality was developed to form DER A. Figure 2 shows the new DER A model. The complete parameter list for the model is given in Table 1. The model has 48 parameters and 10 states, which is roughly 1/3 of the number of parameters of the full large-scale 2nd generation RES generic models [1]. Nonetheless, it preserves a significant number of those features, namely frequency and voltage control emulation, with asymmetric deadband. The voltage control only allows for proportional control, while the model also allows for constant power factor and constant Q-control. It is possible, however, that both constant Q-control and proportional voltage control or constant power-factor (pf) control and voltage control are in effect simultaneously. For example, assume the distributed generation is in constant Q-control, holding a small lagging power factor (or in constant pf-control at a small lagging pf), such that it is generating 0.1 MVAr on a 2 MVA unit. Then assume that Kqv = 10 (proportional voltage control gain) and dbd1 = dbd2 = 0.05 with Vref0 = 1.0. Now so long as the voltage remains within 0.95 to 1.05 pu, the Q output of the unit remains at 0.1 MVAr. If an event occurs to depress the



Figure 2: The distributed energy resource model version A (DER A)

voltage or raise the voltage outside of the deadband, then the proportional control will act to increase/decrease Q until the voltage comes back inside the deadband, at which point Q drops back to its initial value. This is in keeping with the main proposed concepts in IEEE Standard 1547, though it is not an exact implementation of any specific control strategy. There are of course other possible control strategies, but this model being an implementation of aggregated behavior, the group consensus was to keep it in the simplest format.

This model is intended primarily to be used as an aggregated model of a large number of distributed generators. Thus, the parameters Vrfrac, vl0, vl1, vh0, vh1, tvl0, tvl1, tvh0 and tvh1 collectively allow for emulation of partial tripping of the aggregated model. This is explained in detail, per the pseudo code for this function in the appendix, and associated Figure 3. In this case the linear drop-off (shown in Figure 3) is intended to emulate the gradient of voltage along the feeder. The purpose of these timers is to allow for the emulation of inverters disconnecting under low (or high) voltage scenarios. For example, legacy technology may disconnect quickly for a small voltage dip (i.e. one may set vll = 0.9 and tvll = 0.1 s) while part of the aggregate model may be representing modern inverters that comply with newer standards where it will not disconnect unless the voltage drops significantly for a longer duration (e.g. one may set vl0 = 0.5 and tvl0 = 1 s). Thus, this is to allow for testing various aspects of standards such as IEEE Std 1547 requirements and California Rule 21.

For the emulation of primary-frequency response in *DER_A*, the feedback signal (*Pgen*) is taken from the power-order (*Pord*) and not the terminal of the model (see Figure 2). This is because, in steady-state with frequency at its nominal value, the error into the proportional-



(the code for this logic is provided in the Appendix)

integral controller (*Kpg, Kig*) is zero. The power reference *Pref* will initialize to *Pord*, and the frequency error is zero. Now if *Freq_flag* = 1 and a fault occurs nearby which results in partial tripping of the "aggregated" DER through the action of the *Vrfrac* logic, then the terminal electrical power of DER_A will go down. Thus, if the terminal electrical power is fedback, then the error into the proportional-integral controller (*Kpg, Kig*) would now become positive and Pord will increase until it hits *Pmax*, or until the electrical power output of the model is again equal to *Pref*. This is not appropriate, since there has been no system frequency deviation and also the model should not attempt to restore the power lost due to partial tripping effected by *Vrfrac*. Therefore, by taking the



Figure 4: Frequency tripping logic.

power feedback from the power-order (*Pord*) prior to the Vrfrac block, this problem is avoided. This ensures that *Pord* is always equal to *Pref*, which is what is desired. Furthermore, the user should be allowed to set *Tpord* and *Tp* to zero (0). By doing so and setting Kpg = 0 and using a non-zero value of *Kig*, a simple proportional only droop-control can be effected, since the closed loop around Pord in this case, i.e. when Tpord = Tp = 0, *Kig* cannot be set to zero, it must be a positive number. For similar reasons, the feedback to the power factor controller is also from *Pord*.

The frequency tripping is modeled in simple terms. If frequency goes below *fl* for more than *tfl* seconds, then the entire model will trip. If frequency goes above *fh* for more than *tfh* seconds, then the entire model will trip. This block is disabled, if voltage is below *Vpr*, to avoid tripping on frequency spikes (as calculated in simulation) due to sudden voltage drops. This is depicted in Figure 2, and shown in more detail, in an expanded view, in Figure 4.

The model may also be used to emulate inverter-interfaced distributed energy storage. This is achieved by allowing the model to absorb, as well as generate, real power. The additional flag, *typeflag*, achieves this. When *typeflag* is set to 0, meaning the device is a generator, *Ipmin* (that is, the minimum active current limit) is set to zero. When *typeflag* is set to 1, meaning the device is a storage device, *Ipmin* is set to *-Ipmax*. Need-less-to-say, for the sake of simplicity, there is no attempt to model the storage mechanism (e.g. charging/discharging of a battery) and so it is assumed that the model would only be used for transient simulations (e.g. 10 to 30 seconds) during which there would be no appreciable effect of the storage mechanism.

A simple representation of the voltage source interface that is employed by most equipment vendors (based on [6]) is also modeled, since by far the majority of inverters used for inverter-based resources are current-regulated voltage-source converters.

The details of initializing the model can be found in the

WECC model specification document [7] but the most salient points are summarized here for completeness. The values of Vt and Pgen are the voltage and electrical power at the terminals of the DER A model. Upon initialization, Pref and Qref will be determined in software to properly initialize the model. If Kqv is non-zero, then upon initialization *dbd1* < *Vt* - *Vref0* < *dbd2*, where *Vref0*, dbd1 and dbd2 are user defined value. If this condition is not met, then the software tool will force Vref0 = Vtand indicate this to the user in a warning message. If dbd1 = dbd2 = 0 (which should typically not be done, since these distributed generation models are not intended to tightly control voltage) and Kqv is non-zero, then the program should give a warning/error message to the user and indicate that Vref0 has been set to equal to Vt (to force the error to zero and thus the output of the voltage leg to zero); the initial Q from power flow is then initialized off of the constant Q/pf leg. This is the simplest solution in this case. Finally, during initialization, the software program should check to ensure that the terminal voltage (Vt) of the model initializes to a value that is greater than vl1. Also, vl1 must be greater than or equal to vl0. If either of these conditions are not met, the program will present an error message to the user indicating that the value of vll and vl0 are inappropriate, and thus the model will ignore the Vrfrac block. A similar check should be made on vh1 and vh0. Also, a check should be made to ensure that tvl1, tvl0, tvh1 and tvh0 are all greater than or equal to zero. There is no limitation on which of these timer values should be greater or smaller. The Vrfrac block is explained in more detail in the appendix.

There is a possible control problem. If this model were used to model a single large inverter-based device connected to a weak grid point (i.e. low short-circuit ratio) where the voltage is highly affected by this device, then there could be a possibility for limit-cycling (i.e. voltage goes outside deadband, device brings voltage inside deadband by changing Q, Q drops to constant initial value once voltage is within the deadband, voltage goes outside



Figure 5: Benchmarking test case model.

deadband, etc.). For this, and other reasons, it is in general, not recommended that this model be used to model large plants.

Two other important notes should be made. First, that the filtered value of voltage (Vt_filt) and frequency (Frq_filt) is used in all the controls and timers. Second, that the current limit is modeled as follows:

- a. Q-priority: Iqmax = Imax; Iqmin = -Imax; $Ipmax = \sqrt{Imax^2 \square Iqcmd^2}$; if typeflag = 0 then Ipmin = 0, else Ipmin = - Ipmax
- b. P-priority: Ipmax = Imax; $Iqmax = \sqrt{Imax^2 \square Ipcmd^2}$; Iqmin = -Iqmax; if typeflag = 0then Ipmin = 0, else Ipmin = -Ipmax

A final note is that the post-fault rate of recovery on activecurrent (*rrpwr*) is also imposed (in the opposite direction) when the model is being used to "emulate" charging of an energy storage device. That is, when *Pgen* is negative, then *rrpwr* is applied with its sign changed and it becomes the ramp-rate at which charging power (power being absorbed by the model) increases after a fault.

3. Testing the DER_A Model in Four Commercial Simulation Platforms

Once the model was defined and agreed to, four major commercial software vendors in North America, decided to graciously implement the model in their respective software tools so that it could be tested. This testing was done in two steps. First, a beta version of the model was released by all the software vendors and a set of test protocols were defined [8]. The tests aimed, to the extent possible, to test all the features of the model and ensure that they performed as expected, as well as to benchmark the model across the four commercial platforms to ensure consistent implementation and performance across all the software tools. A simple test case was developed for performing simulations in all the various software platforms, it is shown in Figure 5. A complete list of all the tests and results may be found in a report by the Electric Power Research Institute (EPRI) [8]. These tests were focused on testing the DER A model as a standalone model. The testing proved successful and so the model



Figure 6: Plots from one of the benchmarking tests - Test 1A - voltage sag with a ramped recover.





Figure 7: Simulation results form a large system model (WECC system) where the distributed generation is represented within the composite load model first using the old PVD1 model and then using the new DER_A model.

was approved and released on all the software tools. Figure 6 shows one example of the many tests performed. This testing was lead and performed by EPRI. During the testing one case was found to have some small, but noticeable, difference in response among the tools, where two of the tools matched and the others had a slight difference. This was for the case of playing into the model a frequency wave-form. Upon closer investigation, it was identified that the differences were due to numerical precision of the integration schemes, and thus for now this was not further investigated. Some of these subtle differences in the frequency calculation can actually be seen in the frequency traces in Figure 6.

The next step in testing the model was to incorporate it into the composite load model (Figure 1) and to then test it by using the model to simulate distributed generation across a large system. This testing was done by one of the task force members [9], by taking a WECC base case and simulating some major system events in one region with (i) all the distributed generation initially modeled using the old *PVD1* model [4], and (ii) by replacing all the *PVD1* models in the composite load model with the newly developed *DER_A* model. Furthermore, some sensitivities were performed on the model parameters. Example plots from this work are shown in Figure 7. The conclusions that may be drawn from this analysis, as seen in Figure 7, are as follows:

- 1. The *DER_A* model seems to perform well in a large system model.
- 2. If the parameters of the *DER_A* are properly adjusted, it can be made to emulate the older, and much simpler, *PVD1* model this can be seen by the fact that the brown and blue lines in the simulations (Figure 7) match for the total net load and distributed generation in the area, which is driven by the performance of these models.
- 3. Having the DER modeled as a part of the composite



load becomes more critical with the higher penetration of the behind-the-meter distributed generation. The earlier and simpler models for these resources may potentially give less accurate and less realistic results since they do not have the time constants and timedependent tripping logic in the *DER_A*. This can be seen by the fact that in the simulations the green lines (where the time constants in the *DER_A* model have been varied to more closely mimic rule 21) show significantly different total distributed generation response as compared to the brown/blue lines (where the *PVD1*, and *DER_A* made to mimic *PVD1*, model is used).

4. Additional research is needed to better understand how to parameterize the *DER_A* model, to perform sensitivity studies to understand the sensitivity of study results to the various parameters and thus which parameters are most critical.

4. Conclusions and Future Work

A new proposed distributed energy resource model has been presented here. This model has now been adopted by several commercial software vendors in North America, and more recently by at least one software vendor in Europe. It has been shown, through testing the model in four of the commercial software tools that consistent and appropriate results can be obtained across the software tools. Furthermore, initial simulations in a large system model have shown reasonable results as well as consistency with the older, and simpler models.

All of the above said, the task force that developed this model fully realizes the following challenges and ongoing research and development that is needed:

- To perform research on how to best/better parametrize the model to suitably represent the aggregated behavior of distributed generation in a system for both (i) existing distributed generation, and (ii) for future planed distributed generation.
- To look at the sensitivity of large system simulation results to the various parameters of this aggregated model in order to better understand the sensitivity of system performance to the various model parameters. Such work may lead to identifying aspects of the model that need to be refined or changed in the future in order to better model the actual aggregated behavior of distributed generation. Thus, it is fully understood

that the model as it stands may have limitations and there may be aspects that require refinement as greater experience is gained with distributed generation and as the technologies evolve.

• To look more closely at the frequency response capability modeling within the *DER_A* model. This aspect has not been fully tested and may not be fully representative of the aggregate response of distributed generation. To date, to our knowledge, there is no deployment of distributed generation in North America with primary frequency response capabilities, and so this will require further and future work to more properly test and refine in the *DER_A* model.

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Table 1: Model parameter list

Parameter	Description
Trv	transducer time constant (s) for voltage measurement
Trf	transducer time constant (s) for frequency measurement (must be ≥ 0.02 s)
dbd1	lower voltage deadband ≤ 0 (pu)
dbd2	upper voltage deadband ≥ 0 (pu)
Kqv	proportional voltage control gain (pu/pu)
Vref0	voltage reference set-point > 0 (pu)
Тр	transducer time constant (s)
Tiq	Q control time constant (s)
Ddn	frequency control droop gain ≥ 0 (down-side) (pu/pu)
Dup	frequency control droop gain ≥ 0 (up-side) (pu/pu)
fdbd1	lower frequency control deadband ≤ 0 (pu)
fdbd2	upper frequency control deadband ≥ 0 (pu)
femax	frequency control maximum error ≥ 0 (pu)
femin	frequency control minimum error ≤ 0 (pu)
Pmax	Maximum power (pu)
Pmin	Minimum power (pu)
dPmax	Power ramp rate up > 0 (pu/s)
dPmin	Power ramp rate down < 0 (pu/s)
Tpord	Power order time constant (s)
Крд	active power control proportional gain (pu/pu)
Kig	active power control integral gain (pu/pu/s)
Imax	Maximum converter current (pu)
vl0	voltage break-point for low voltage cut-out of inverters (pu)
vl1	voltage break-point for low voltage cut-out of inverters (pu)
vh0	voltage break-point for high voltage cut-out of inverters (pu)
vh1	voltage break-point for high voltage cut-out of inverters (pu)
tvl0	timer for vl0 point (s)
tvl1	timer for vl1 point (s)
tvh0	timer for vh0 point (s)
tvh1	timer for vh1 point (s)
Vrfrac	fraction of device that recovers after voltage comes back to within vl1 < V < vh1
fl	frequency break-point for low frequency cut-out of inverters (pu)
fh	frequency break-point for high frequency cut-out of inverters (pu)
tfl	timer for fl (Tfl > Trf) (s)
tfh	timer for fh (s)
Tg	Current control time constant (s)
rrpwr	Power rise ramp rate following a fault > 0 (pu/s)
Τv	time constant on the output of the voltage/frequency cut-out (s)
Vpr	voltage below which frequency tripping is disabled (pu)
Pflag	0 - for constant Q control, and 1 - constant power factor control
Pqflag	0 - Q priority, 1 - P priority for current limit
Freq_flag	0 - frequency control disabled, and 1 - frequency control enabled
Ftripflag	0 - frequency tripping disabled; 1 - frequency tripping enabled
Vtripflag	0 - voltage tripping disabled; 1 - voltage tripping enabled
typeflag	0 - the unit is a generator Ipmin = 0; 1 - the unit is a storage device and Ipmin = - Ipmax
Xe	Source impedance reactive > 0 (pu)
lqh1	Maximum limit of reactive current injection (pu)
lql1	Minimum limit of reactive current injection (pu)



6. Appendix: Pseudo code for the *Vrfrac* block.

The block shown in Figure 3 is implemented consistent with the existing PVD1 model, as described in a WECC report [4]. However, the pseudo code and logic here is quite different to that in [4], since we have added two (2) time parameters tvl0 and tvl1, which determine when the limits are imposed once the assigned time has lapsed. That is, the output of the block will always track the path of the black line in Figure 3, unless certain conditions are met. If the voltage stays below *vl1* for a duration greater than *tvl1*, then it will now always follow the path of the red line when the voltage recovers. If the voltage stays below *vl0* for greater than *tvl0*, then the output will always remain at zero. In order to reduce this block back to that implemented in PVD1, one would have to set Trv = 0(eliminate the filtering of voltage) and set *tvl0* = 999, *tvl1* = 0.0, tvh0 = 999, and tvh1 = 0.0.



Figure 8: Understanding how Vmin is determined.

Note that Vmin in Figure 3 is not an input parameter, it is an internal software variable which is keeping track of the minimum voltage that the terminal of the model reaches during a simulation, immediately after the timer *tvl1* times out. That is, *Vmin* is the lowest point of *Vt* during a simulation, but at the moment that timer *tvl1* times out it is set to (and kept at) the value of *Vt* at that instant. This is done to avoid jumps in the response due to movement (oscillations) in voltage. For example, consider the following scenario. During an event *Vt* goes down to *Vmin_a*, then comes back up to *Vt_2*, and then goes again down to *Vmin_b*, at which time the timer for tvl1 times out. Thus, it is the value of *Vmin_b* which we would like *Vmin* to be set to. This is depicted below in Figure 8.

Vmin should initialize to the initial value of *Vt* or a default value (e.g. 1.0).

```
Timer 1 = 0
Timer 2 = 0
Counter 1 = 0
Counter 2 = 0
If Vt < vl1 and Timer 1 = 0
        Start Timer 1
elseif Vt > vl1 and Timer 1 started
        Reset Timer 1
end
If Vt < vl0 and Timer 2 = 0
        Start Timer 2
elseif Vt > vl0 and Timer 2 started
        Reset Timer 2
end
if Vmin <= vl0
Vmin = vl0
end
if Vt \leq vl0 or Counter 2 = 1
Multiplier = 0.0
elseif Vt \leq vl1 and Counter 1 = 0
```

Multiplier = (Vt - vl0) / (vl1 - vl0)

elseif Vt \leq vl1 and Counter 1 = 1



```
Multiplier = ((Vmin - vl0) + Vrfrac * (Vt - Vmin)) / (vl1 - vl0)
```

elseif Vt \geq vl1 and Counter 1 = 0

Multiplier = 1

```
else
```

 $\begin{aligned} \text{Multiplier} &= \text{Vrfrac} * \left((\text{vl1} - \text{Vmin}) / (\text{vl1} - \text{vl0}) \right) + \left((\text{Vmin} - \text{vl0}) / (\text{vl1} - \text{vl0}) \right) \end{aligned}$

```
end
```

```
if Counter 1 = 0
```

if Timer1 > tvl1

```
Counter 1=1
```

```
Vmin = Vt
```

```
end
```

end

if Counter 2 = 0

if Timer2 > tvl0

Counter 2=1

end

end

The key here is that Counter 1 (2) get set only if the condition of being below vll (vlo) is met for the given time duration and once that condition is met the block remains in that state indefinitely. Also, *Vmin* is set to the value of Vt at the point when timer 1 (tvll) times out.

The same logic is then implemented for *Vt* exceeding vh1 while keeping track of the maximum voltage reached during the simulation (*Vmax*) (see *Vrfrac* in Figure 2).

Note that if in a single simulation both a voltage dip and a voltage rise is experienced, then the two arms of the *Vrfrac* block simply multiply by each other. That is, for example, if one first goes into a voltage dip, then coming out of the dip the total magnitude of the block is affected by *Vrfrac*, as determined by the results of the voltage dip. This then becomes the value that goes into the voltage rise scenario and is then affected by the *Vrfrac* determined by the voltage rise logic.

7. Biographies

Pouyan Pourbeik received his BE and PhD in Electrical Engineering from the University of Adelaide, Australia in 1993 and 1997, respectively. From 1997 to 2000 he was with GE Power Systems. From 2000 to 2006 he was with ABB Inc. From 2006 to March, 2016 he was with EPRI. From April, 2016 he is with Power and Energy, Analysis, Consulting and Education, PLLC. He is an Honorary Member of CIGRE and a Fellow of the IEEE, and a past chairman of both CIGRE Study Committee C4 – System Technical Performance, and the IEEE PES Power System Dynamics Performance Committee.

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