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SIPROTEC 4 Application Note

SIP4-APN:
Circulating Current High Impedance Differential Protection Using Multifunctional Relay 7SJ6
Edition 2014-10-17

Answers for energy management.

SIPROTEC 4 - Application:
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Circulating Current High Impedance Differential Protection
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Content

1 Introduction 4
2 Circulating Current High Impedance Protection 5
2.1 General Remarks regarding High Impedance Protection Schemes 5
2.2 High Impedance Protection Scheme Design 5
2.2.1 Relevant primary system data 5
2.2.2 Relevant current transformer data 6
2.2.3 Relevant protection device data and auxiliary component data 6
3 Procedure for High Impedance Protection Scheme Calculations 7
3.1 Relevant data required 7
3.1.1 Establish the relevant power system data 7
3.1.2 Establish the relevant current transformer data 7
3.1.3 Establish the relevant relay data and necessary auxiliary component elements 8
3.2 Calculation of the minimum required stabilizing voltage 10
3.3 Calculation of the required fault setting 10
3.4 Calculation of the required stabilizing resistor 11
3.5 Calculation of the required non-linear resistor (varistor) 11
3.6 Calculation of the required thermal ratings of the auxiliary components: stabilizing resistors and varistors 12
3.6.1 Thermal rating of varistor 12
3.6.2 Thermal rating of stabilizing resistor 14
3.7 Final check of the scheme sensitivity 15
4 Working Example 16
4.1 Relevant data required 16

4.1.1 Relevant power system data 16
4.1.2 Relevant current transformer data 16
4.1.3 Relevant relay data and necessary auxiliary component elements 16
4.2 Calculation of the minimum required stabilizing voltage 17
4.3 Calculation of the required fault setting 17
4.4 Calculation of the required stabilizing resistor 17
4.5 Calculation for the required non-linear resistor (varistor) 18
4.6 Final check of the scheme sensitivity 19
4.7 Scheme settings 20
4.7.1 CT supervision 20
4.8 Connection Example 21
5 Applications 22
5.1 Phase and earth-fault high impedance differential protection of busbars 22
5.2 Phase and earth-fault high impedance differential protection of auto-transformers 22
5.3 Phase and earth-fault high impedance differential protection of motors or generators (synchronous) 23
5.4 Phase and earth-fault high impedance differential protection of series reactors 23
5.5 Phase and earth-fault high impedance differential protection of shunt reactors 23
5.6 Restricted earth fault (REF) protection schemes of transformer windings 24
6 References 25

1 Introduction

Three-phase (phase-segregated) circulating current high impedance protection schemes are typically applied for the following protection objects: busbars, auto-transformer, series reactor, shunt reactor or even to motors or generators. Regarding busbars arrangements, the high impedance protection scheme is widely used for arrangements like single busbars, single busbars with sectionalizer, or circuit-breaker-and-a-half arrangements. The usage of high impedance busbar protection for double busbars is not recommended, because of high complexity related to switching-over of CT secondaries that decreases the scheme reliability.

Single-phase restricted earth fault (REF) protection schemes may be used in principle to all the protected object as listed above, but the most common application is to protect transformer windings which are earthed via impedance, solidly earthed or even for transformer winding connected in delta (in this case the scheme is sometimes called high impedance balanced earth fault).

The multifunctional relay 7SJ6 can be used within all the mentioned high impedance protection schemes, both in phase-segregated circulating current high impedance protection applications, as well as in single phase restricted earth fault protection applications.

This document provides description of the multifunctional relay 7SJ6 application in phase-segregated circulating current high impedance protection scheme. Thereby the guideline for the calculations related to the high impedance differential protection schemes is described together with the comments on the relay setting parameters.

Description of the single-phase high impedance restricted earth fault protection applications is already included within the relay manual; therefore it will be omitted in this guide.

2 Circulating Current High Impedance Protection

2.1 General Remarks regarding High Impedance Protection Schemes

In contrary to the low impedance differential protection schemes, where each of several CTs forming differential protection zone is directly connected to a separate relay input, the high impedance protection scheme is formed by the parallel connection of all CTs secondaries within a given protection zone (Figure 1).

While low impedance protection schemes evaluate signals within the relay that come from each of the CTs independently, the relay in the high impedance scheme evaluates the current that results from the interaction of all the involved CTs as it flows in the differential branch (Figure 1).

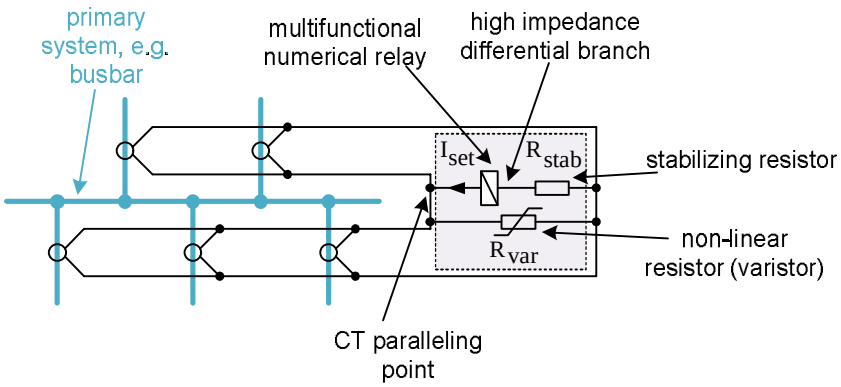

Figure 1 Typical connection of elements within a high impedance differential protection scheme

Thereby, the stability of the differential scheme on CT saturation plays in all schemes an important role.

Low impedance protection schemes evaluate CT secondary currents which may be saturated by their high burden and/or high secondary currents. Thereby, multiple CT currents are evaluated by relay (nowadays relay software), whereas each CT saturates independently from the others, i.e. the CTs do not influence each other in their performance. Therefore, in the low impedance differential protection devices several different stabilizing measures and algorithms for better stability and selectivity are applied.

Within a high impedance scheme the CTs do influence each other, as all of them are connected in parallel (Figure 1). The stabilization against CT saturation is realized by the placement of an extra element (hardware), namely the stabilizing resistor so no further measures against CT saturation have to be implemented in the relay. Therefore, the relay used within the high impedance protection scheme can be of over-current relay type without involving any additional measures against CT saturation. All the other high impedance scheme performance quantities: as required fault sensitivity, scheme stability are then dependent on the scheme design involving adequately chosen CT parameters and auxiliary components (stabilizing resistor, varistor) that suit given application.

2.2 High Impedance Protection Scheme Design

2.2.1 Relevant primary system data

Protection object characteristic has major influence on the protection scheme design. Therefore, typically the following properties shall be known

- Short-circuit fault level including:
  - maximum symmetrical short-circuit withstand current of the switchgear
  - maximum symmetrical short-circuit current for external (through) faults
  - maximum symmetrical short-circuit current for internal faults
  - minimum symmetrical short-circuit current for internal faults

For the latter ones especially neutral earthing conditions (earth-fault limitation) shall be considered, as well. Moreover, all the above currents can be three-phase, double-phase or phase-to earth depending on the application/protected object.

- Rated parameters of the protected object including
  - rated power, resp. rated current, impedance voltage, sub-transient reactance, ...
- Rating of the primary switching elements like circuit breaker, isolators within the switchgear that are relevant to the protected object

2.2.2 Relevant current transformer data

The prerequisite (a must) to high impedance schemes is that all the involved CTs have to have the same current ratio. The usage of CTs as per IEC 61869-2 Standard [1] class PX (former BS class X) is generally recommended. Those CTs have current ratio error limitation and are of low-leakage type. However, for some high impedance protection schemes involving less number of CTs (e.g. REF) also CT of IEC 61869-2 class 5P can be used. Thereby, their current ratio error as well as the respective magnetizing curves together with internal resistances shall be known. Also CTs of the former (now obsolete) IEC 44-6 class TPS can be used within high impedance protection applications. Hereby, it is recommended to transfer their nameplate parameters to the respective IEC class PX parameters. For high impedance busbar protection SIEMENS recommends usage of IEC class PX cores. The following relevant CT parameters shall be known:

- CT nameplate data (preferably confirmed by test protocols)
  - CT ratio
  - CT knee-point electromotive force (emf)[1]
  - CT exciting current at the knee-point emf
  - CT secondary winding resistance at 75 ^{O}C
- CT secondary wiring resistance from the CT clamps to the paralleling point of the scheme (loop resistance)
- Number of CTs that belong to the differential protection zone

Remark: Regarding knee-point emfs, exciting currents and secondary winding resistances of the used CTs it can be stated that small deviations between the used CTs can be typically tolerated without negative influence on the scheme performance. The scale of deviation and its influence on the scheme design and performance, however, shall be analyzed on a case basis.

2.2.3 Relevant protection device data and auxiliary component data

For the high impedance scheme design the relay operating (settable) current range shall be known, so that it can suit the application with regard to the fault sensitivity. The burden of the relay input is typically very small comparing to external stabilizing resistance and can in most applications be neglected.

Remark: In the past the relays used constant operating current (e.g. 20 mA or 100 mA) and the setting was adjusted by settable resistors (mounted internally within the relay). Very often such relays were named 'voltage operated'. Nowadays, modern digital protection relay with wide range settable current setting are used. This gives additional flexibility for covering several high impedance protection applications using one type of the relay. The auxiliary component like resistors and varistors are then typically installed separately within the protection cubicle.

Further chapters guide on relevant calculations and propose scheme design for using multifunctional relay 7SJ6 within high impedance differential protection schemes.

[1] Definition as per IEC 61869-2 ; in practice the term 'knee point voltage' is widely used for this quantity. However, as per standard the term knee point voltage describes rather the voltage that is applied to the secondary terminals of the CT during testing. For the sack of the standard compatibility and correctness the term emf will be used through this application guide.

3 Procedure for High Impedance Protection Scheme Calculations

This chapter provides remarks on scheme design and a guide for the scheme relevant calculations.

3.1 Relevant data required

3.1.1 Establish the relevant power system data

At first the power system primary data that are relevant to the protected object shall be collected.

1. From the scheme stability and thermal design of components point of view the following relevant power system information shall be known:
   - the maximum symmetrical short-circuit current for external (through) faults $I''_{sc,max,ext}$
   - the maximum symmetrical short-circuit current for internal faults $I''_{sc,max,int}$

   Remark: In case of a busbar, the maximum short-time symmetrical short-circuit withstand current of the switchgear $I''_{sc,max,swg}$ may be considered for both of the above quantities.
2. From the scheme sensitivity and relay setting range point of view the following relevant power system information shall be known:
   - the rating of the feeder /diameter circuit breakers or maximum prospective load on those feeders $I_{r,load}$
   - the minimum symmetrical short-circuit current for internal faults $I''_{sc,min,int}$

   Remark: In power systems with solidly (effectively) earthed neutral-points, the double-phase fault is typically the smallest one and it can be typically considered here. In power systems with earth-fault current limitation (neutral point of power transformers is not directly earthed) the single-pole fault current shall be considered. However, for busbar protection schemes in networks with strongly limited earth fault current (e.g. to several Amps in medium voltage networks with presence of rotating machines) there is often not necessary to detect the earth-fault using such scheme.

3.1.2 Establish the relevant current transformer data

As previously mentioned the CTs used in the high impedance schemes shall be with equal ratios, of low leakage type and with limited current ratio error. For high impedance busbar protection SIEMENS recommends usage of IEC class PX CTs.

At first:

- the number of CTs that belong to the considered /designed differential protection zone N_{CT}

shall be known, and for each of these CTs their respective IEC class PX [1] parameters shall be collected :

- CT Ratio, $k_r = \frac{I_{pr}}{I_{sr}}$ where I_{pr} and I_{sr} are primary and secondary rated current, respectively
- rated CT knee-point emf E_k
- CT exciting current at the knee-point emf I_e
- CT secondary winding resistance R_{CT} (d.c. resistance corrected to 75 ^{O}C)

Remark: The values of knee-point emf and the respective exciting current can be obtained / read from the magnetizing characteristic or testing protocols. Both values shall be rms-values, as per IEC class PX.

Furthermore for each CT:

- the resistance of secondary wring from the CT clamps to the paralleling point of the scheme (loop resistance) R_{wire}

  Remark: The wiring resistances are either given in the tender documentation or can be calculated from the layout drawings of the switchgear. Typically, a maximum wiring resistance can be estimated and specified as a maximum allowable for the worst case considerations.

3.1.3 Establish the relevant relay data and necessary auxiliary component elements

At first the type of the relay input that will be used shall be known and its respective:

- operating current setting range $I_{\text{set,range}}$,
- burden of the relay input used, typically expressed as resistance R_{relay} .

Regarding the first one, it is proposed to activate the following device configuration function in the multifunctional relay 7SJ6:

0112	DMT / IDMT Phase	Definite Time Only

Furthermore within Setting Group A ;
Group DMT / IDMT Phase/Earth Overcurrent /General the following is proposed to activate:

1201	Phase Time Overcurrent	ON

All other parameters being OFF.

Then, within Group DMT / IDMT Phase/Earth Overcurrent /DMT Ph, the stage I>>> shall remain disabled (OFF). E.g.:

1219A	I>>> measurement of	Fundamental component	
1216A	I>>> active	Always	
1217	I>>> Pickup	oo A (OFF)	Range: 1A ...35A, stps. 0.01A
1218	I>>> Time Delay	oo sec (OFF)	Range: 0s ...60s, stps. 0.01s

The stage I>> shall be activated for the main function (high impedance protection trip) with the following settings (please note: trip setting shown below –address 1202 and 1203 – is exemplarily only):

1220A	I>> measurement of	Fundamental component	
1214A	I>> active	Always	
1202	I>> Pickup	0.5 A (e.g. I_{set})	Range: 0.1A ...35A, stps. 0.01A
1203	I>> Time Delay	0.0 sec (Trip)	Range: 0s ...60s, stps. 0.01s

Depending on application the I> stage can be then used for CT supervision purposes or switched OFF in case when external supervision relay is used (this depends on customer practice)

1221A	I> measurement of	Fundamental component	
1204	I> Pickup	0.1 A (e.g. I_{superv})	Range: 0.1A ...35A, stps. 0.01A
1205	I> Time Delay	5.0 sec (e.g. superv.)	Range: 0s ...60s, stps. 0.01s

Remark: The usage of flexible functions within the multifunctional relay is also possible for high impedance differential protection. Thereby, the usage of single function with one common setting for the three phases and a common trip command is proposed. Care must be taken, that the setting for 'Selection of Measurement Method' for the current measurement shall be always set to 'Fundamental component'. For CT supervision requirements, a second stage of flexible functions can be used, issuing an alarm after supervision time has elapsed and releasing CT shorting relay.

The actual burden of multifunctional digital relay 7SJ6 can be taken from the relay manual (chapter technical data, 4.1.1):

R_{relay} = 0.05 Ω.

4.1.1 Analog Inputs

Current Inputs

Nominal Frequency	f_{Nom}	50 Hz or 60 Hz	(adjustable)
Nominal Current	I_{Nom}	1 A or 5 A	
Ground Current, Sensitive	I_{Ns}	≤ linear range 1.6 A [1)]	
Burden per Phase and Ground Path - at I_{Nom} = 1 A - at I_{Nom} = 5 A - for sensitive ground fault detection at 1 A		Approx. 0.05 VA Approx. 0.3 VA Approx. 0.05 VA	

Furthermore, the relay 7SJ6 requires always external equipment to build the high impedance protection scheme. This equipment consist typically of stabilizing resistor (-s) for setting up the respective scheme stabilization and non-linear resistor (-s) , i.e varistor (-s) to protect whole secondary equipment against overvoltages (i.e. CTs secondaries, the differential branch and the wirings). Typically per phase (per one relay input) one stabilizing resistor and one varistor is necessary.

The design and selection of these elements is subject of the scheme calculations (as shown in next chapters).

Remark: For busbar protection schemes which are equipped with CTs with high knee-point emfs, the presence of varistor is mandatory to protect the secondary equipment and wiring against high voltages that may appear during internal faults (see also calculations in item 3.5).

The presence of further relays e.g. for CT supervision, CT shorting, circuit breaker lock-out and/or test switches depends on respective customer practice.

3.2 Calculation of the minimum required stabilizing voltage

The prerequisite of a proper designed high impedance scheme is its stability to external faults. That means that protection relay installed in the differential branch must remain stable under maximum through fault conditions, when a voltage $U_{\text{diff,ext}}$ is developed across the differential branch due to high fault current and CT saturation.

This maximum prospective voltage $U_{\text{diff,ext}}$ can be practically calculated on a safe side assuming full CT saturation of one of the CTs within the scheme and considering the highest values of R_{CT} and R_{wire}. Taking the above into account, this voltage can be calculated as per Eq (1) and then taken as the minimum required stability voltage of the high impedance scheme U_{stab}:

$$U_{\text{stab}} = U_{\text{diff,ext}} = \frac{I_{\text{max,ext}}}{k_{\text{r}}}\left(R_{\text{CT}} + R_{\text{wire}}\right) \tag{1}$$

Remark: It is recommended that the differential branch is installed at the electrical mid-point of the system, i.e. the resistances R_{CT} and R_{wire} of all branches should be equal or similar. Slight deviations of R_{wire} can be typically tolerated but it must be kept in mind that these lead to an unbalance in the system during load conditions and in consequence may lead to an unnecessary energy dissipation (heating) at auxiliary scheme elements like stabilizing resistors. Also slight deviations of R_{CT} values between CTs used in a scheme can be tolerated. For most practical cases 'worst-case' value (highest R_{CT} among all CTs in a scheme) can be used in Eq. (1).

Summarizing, the setting voltage of the scheme U_{set} (in practice this voltage results from the multiplication of the relay current setting and stabilizing resistor value) over the differential branch must be made equal or greater than the required stability voltage (Eq. (1)).

$$U_{\text{set}} \geq U_{\text{stab}} \tag{2}$$

3.3 Calculation of the required fault setting

In further steps the following scheme requirements shall be assured:

a) the functionality (trip on internal fault) and
b) sensitivity of the scheme that suits given application.

Ad a): To assure the first requirement, the CT knee-point emf E_{k} shall fulfill the following requirement:

$$E_{\text{k}} \geq 2 \cdot U_{\text{set}} \tag{3}$$

Remark: Re-writing the Eq. (3)in form

$$U_{\text{set}} \leq E_{\text{k}} / 2 \tag{4}$$

and comparing it to Eq (2):

$$U_{\text{set}} \geq U_{\text{stab}} \tag{5}$$

one may become the minimum and maximum values for the scheme setting voltage. As per our practice it is worthy to keep in mind that the setting voltage U_{set} shall practically not exceed 300 V because this will introduce difficulties in finding the proper auxiliary equipment (like varistors, etc.).

Ad b): In order to reach the desired scheme sensitivity, i.e. to trip on internal fault, the current setting of the relay in the differential branch shall be calculated.

To do that, the desired primary fault sensitivity $I_{\text{p,des}}$ of the scheme shall be chosen at first.

The primary fault sensitivity, (i.e. the value of the primary internal fault current that the protection scheme shall be able to detect) must suit the corresponding application. So its choice depends on the protected object, the minimum fault level and/or the type of neutral point earthing. The choice is typically made by protection engineers according to their practice or e.g. as per ENA standard ([2]). Exemplarily, choosing the primary fault sensitivity for busbars, the rated load of the outgoing feeder $I_{\text{r,load}}$ or rating of the circuit breaker or minimum fault level $I''_{\text{sc,min,int}}$ can be considered.

Having chosen the primary fault sensitivity $I_{\text{p,des}}$ of the scheme, the secondary setting of the relay I_{set} can be calculated bearing in mind that the elements connected together within a high impedance protection scheme will decrease the sensitivity consuming a portion of current at the corresponding scheme setting voltage U_{set} (i.e. exciting currents I_{e} of the CTs, varistor spill current I_{var} at the setting voltage):

$$I_{\text{set}} = \frac{I_{\text{p,des}}}{k_{\text{r}}} - \sum_{x=1}^{N_{\text{CT}}} \frac{U_{\text{set}}}{E_{\text{k,x}}} I_{\text{e.x}} - I_{\text{var}}(U_{\text{set}}) \approx \frac{I_{\text{p,des}}}{k_{\text{r}}} - N_{\text{CT}} \frac{U_{\text{set}}}{E_{\text{k}}} I_{\text{e}} - I_{\text{var}}(U_{\text{set}}) \quad (6)$$

Remark: A rough calculation as per right side of the Eq. (6) is enough for most practical cases. Thereby, often the 'worst-case' CT data are considered, i.e. the lowest E_{k}, the highest I_{e}. This has an influence on the calculated sensitivity, so the real fault sensitivity can differ (is higher in this case). This fact shall be considered when choosing required primary fault sensitivity.

3.4 Calculation of the required stabilizing resistor

With the steps described in items 3.2 and 3.3 the basic properties of the high impedance protection scheme were calculated: the scheme setting voltage U_{set} and the current setting of the relay I_{set}.

The multifunctional relay 7SJ6 requires external stabilizing resistor R_{stab} to be connected in series to the relay input in order to assure the necessary scheme setting voltage U_{set}.

The value of the stabilizing resistor can be calculated in straightforward way using the scheme setting voltage U_{set} and the setting of the relay I_{set}, as chosen in the previous steps:

$$R_{\text{stab}} = \frac{U_{\text{set}}}{I_{\text{set}}} - R_{\text{relay}} \approx \frac{U_{\text{set}}}{I_{\text{set}}} \quad (7)$$

Thereby, the relay input burden R_{relay} can be typically neglected.

3.5 Calculation of the required non-linear resistor (varistor)

As stated in the previous chapters, during an internal fault high voltage may arise across the differential branch (i.e. the tie with relay and R_{stab} connected in series). Therefore, non-linear resistors are necessary in order to avoid secondary circuits (wirings, CT clamps, resistors, etc) be exposed to high voltages. Such varistors shall be connected across the differential branch.

The secondary circuits are typically designed to withstand 3000 V peak. In practice, in order to safely protect secondary circuits of high impedance schemes the usage of a varistor is necessary when the voltage across the differential branch may exceed around 1500 V rms, which is 2121 V peak. That can be rounded down with a safety margin to 2000 V peak.

In order to estimate whether this voltage may appear in the designed scheme, at first the theoretical rms voltage $U_{\text{sc,max,int,rms}}$ which would occur across the differential branch if CT did not saturate shall be determined according to the following equation:

$$U_{\text{sc,max,int,rms}} = \frac{I''_{\text{sc,max,int}}}{k_{\text{r}}}\left(R_{\text{relay}} + R_{\text{stab}}\right) \tag{8}$$

Considering CT saturation, the resulting maximum peak voltage across the differential branch $\hat{U}_{\text{max,tie}}$ can be calculated [2]:

$$\hat{U}_{\text{max,tie}} = 2\sqrt{2E_{\text{k}}\left(U_{\text{sc,max,int,rms}} - E_{\text{k}}\right)} \tag{9}$$

Summarizing, when the relationship in (10) is fulfilled the usage of varistor is mandatory:

$$\hat{U}_{\text{max,tie}} > 2000\,\text{V} \tag{10}$$

Remark: High impedance restricted earth-fault protection applications may sometimes not require varistor, but busbar protection applications in general do. However, it is considered as good practice to equip with a varistor all high impedance protection installations.

The protection level of the varistor can be estimated from its characteristic (for dc or instantaneous values)

$$\hat{U}_{\text{var}} = C \cdot \hat{I}^{\,\beta}, \tag{11}$$

where the constants C and β shall be given by the varistor manufacturer.

The rms protection level is then:

$$U_{\text{var}} \sim \hat{U}_{\text{var}} / \sqrt{2}, \tag{12}$$

3.6 Calculation of the required thermal ratings of the auxiliary components: stabilizing resistors and varistors

The ratings of both components, stabilizing resistor and varistor, shall be then chosen to match the application.

3.6.1 Thermal rating of varistor

The varistor shall be chosen to match the differential branch setting voltage and to limit the voltage to a safe value. i.e. its characteristic must not change significantly for voltages below and beyond the differential branch setting U_{set} up to the voltage limit of e.g. 2000 V peak. The varistor must be also capable of passing the maximum prospective fault current that can be transformed by the CT.

The type of varistor required can be typically chosen by calculating its necessary thermal rating as defined by the following empiric formula:

$$P_{\text{var}} = \frac{4}{\pi} \cdot \frac{I_{\text{sc,max,int}}}{k_{\text{r}}} E_{\text{k}} \tag{13}$$

The absorbed thermal energy during internal short-circuit current flow is then

$$W_{\text{var}} = P_{\text{var}} \cdot t_{\text{sc}} \tag{14}$$

During scheme design one shall determine the maximum duration of fault t_{sc} and calculate the energy dissipation rating using Eq. (14). Since the varistor shall practically withstand the CB-fail or protection fail conditions during an internal fault, the maximum fault clearance time t_{sc} taken as of 1 s is typically sufficient. Therefore, the result of calculation according to Eq.(14) can be compared to 1 second rating of the varistor.

Regarding thermal rating of the varistor the following issues shall be considered:

a) One shall note that in high impedance schemes utilizing CTs with $E_k > U_{var}$ the Eq.(13) provides too large values as they may appear in the real scheme with varistor applied (since the varistor becomes low-ohmic at voltages below E_k, leading to the fact that CTs do not saturate, so the amount of energy delivered to the scheme is then limited not by the knee-point emf but by the varistor protection voltage U_{var}). In such cases it is proposed to estimate the thermal rating according to the empiric formula (15):

$$P_{var,mod} = \frac{4}{\pi} \cdot \frac{I_{sc,max,int}}{k_r} U_{var} \text{ , for } E_k > U_{var} \quad (15)$$

b) Furthermore, the calculation of thermal rating of the varistor does not include the energy absorption by the stabilizing resistor during an internal fault.

c) However, in case when varistor will be taken out of operation (damaged, etc.), the energy as per Eq.(13) will appear and dissipate on the stabilizing resistor alone. This issue can be considered by choosing (limiting) knee point emfs of the CTs.

d) the calculation as per Eq.(13) can be seen as being on the safe side, as long as the real (measured) E_k of the CT is known. Care shall be taken to cases when nameplate data of E_k is used. As per IEC standard [1] the E_k on the nameplate is the minimum value, which can be (even considerably) smaller than the real (measured) knee-point emf.

In addition to the thermal rating of the varistor the following recommendation shall be fulfilled:

1. At setting voltage of the scheme U_{set} the varistor rms current I_{var}, calculated as per Eq.(16) shall not exceed 30mA in high impedance schemes utilizing CTs with 1 A secondary rated current, and 100mA in high impedance schemes utilizing CTs with 5 A rated current (not recommended).

$$I_{var} = 0.52 \cdot \left(\sqrt{2} \cdot \frac{U_{set}}{C} \right)^{1/\beta} \quad (16)$$

Summarizing the above, in most cases this practically leads to a choice between two main types of varistor available from e.g. Metrosil for high impedance schemes utilizing CTs with 1 A secondary rated current, as shown in Table 1.

Table 1 Proposed Metrosil varistor types for high impedance circuits with 1 A secondary (mostly used)

Metrosil identification (type)	Parameters of the varistor characteristic			Recom. max branch setting voltage U_{set} [Vrms]	Rated energy absorp. for 200°C temp rise W_{var} [J]	Short Time Current [Arms]		
	C	β	α			1s	2s	3s
600A/S1/S256 (single pole) 600A/S3/1/802 (three pole)	450	0.25	0.87	125	53333	45	30	22
600A/S1/S1088 (single pole) 600A/S3/1/S1195 (three pole)	900	0.25	0.87	300	88000	39	23	17

Remark: Also different types / different manufacturers of varistors can be used in high impedance protection applications.

Remark: In high impedance schemes utilizing CTs with 5 A rating (not recommended) different types of varistors may apply.

3.6.2 Thermal rating of stabilizing resistor

The thermal rating of the stabilizing resistor is typically carried out considering the following steps:

At first, the continuous power rating of the stabilizing resistor can be chosen as per (17):

$$P_{\text{stab,cont}} \geq \frac{U_{\text{set}}{}^2}{R_{\text{stab}}} \tag{17}$$

Remark: It shall be noted that in order to keep the resistor healthy during commissioning tests the fault current from the testing equipment should be immediately withdrawn after the device gives a protection trip.

In second step, R_{stab} must have a short time rating large enough to withstand the fault current before the fault is cleared. Thereby, the rms voltage developed across the stabilizing resistor during maximal prospective internal fault $U_{\text{rms,f}}$ is decisive for the thermal stress of the stabilizing resistor. It is calculated according to mathematically derived formula:

$$U_{\text{rms,f}} = 1.3 \cdot \sqrt[4]{E_{\text{k}}{}^3 \cdot R_{\text{stab}} \cdot \frac{I_{\text{sc,max,int}}}{k_{\text{r}}}} \tag{18}$$

The time duration of 0.5 seconds can be typically considered for the stabilizing resistor ($P_{\text{stab,0.5s}}$).

Remark: Longer times as e.g. 1 s may lead to very huge resistors. The consideration of longer times is impracticable, especially taking into consideration that within the scheme also a varistor is applied, which takes over a part of the thermal energy. The considerations presented here are not taking the varistor into account. Therefore, the 0.5 s rating is on a safe side.

Summarizing, the resulting short-time rating $P_{\text{stab,0.5s}}$ shall be then chosen as per Eq. (19):

$$P_{\text{stab,0.5s}} \geq \frac{U_{\text{rms,f}}{}^2}{R_{\text{stab}}} \tag{19}$$

Regarding thermal rating of the stabilizing resistor the following issues shall be considered:

a) One shall note that in high impedance schemes utilizing CTs with $E_{\text{k}} > U_{\text{var}}$ the Eq. (19) provides too large values as they may appear in the real scheme with varistor applied (since the varistor becomes low-ohmic at voltages below E_{k}, leading to the fact that CTs do not saturate, so the amount of energy delivered to the scheme is then limited not by the knee-point emf but by the varistor protection voltage U_{var}). In such cases it is proposed to estimate the thermal rating exchanging $U_{\text{rms,f}}$ in Eq.(19) by $U_{\text{rms,f,mod}}$ calculated according to the empirically verified formula (20):

$$U_{\text{rms,f,mod}} = 1.3 \cdot \sqrt[4]{U_{\text{var}}{}^3 \cdot R_{\text{stab}} \cdot \frac{I_{\text{sc,max,int}}}{k_{\text{r}}}} \text{ , for } E_{\text{k}} > U_{\text{var}} \tag{20}$$

b) Furthermore, the calculation of thermal rating of the stabilizing resistor does not include the considerable energy absorption by the varistor resistor during an internal fault.

c) The distribution of the dissipated energy during an internal fault between the stabilizing resistor and varistor is not linear and depends on varistor protection voltage U_{var} and CTs knee-point emf E_{k} together with stability (setting) voltage of the scheme U_{set}. Simplifying, the higher the ratio U_{var} / U_{set} the more energy will be dissipated on the resistor.

d) However, in case when varistor will be taken out of operation (damaged, etc.), the energy as per Eq. (13) will appear and dissipate on the stabilizing resistor alone. This issue can be considered by choosing (limiting) knee point emfs of the CTs.

e) the calculation as per Eq.(19) and respective Eq. (18) can be seen as being on the safe side, as long as the real (measured) E_{k} of the CT is known. Care shall be taken to cases when nameplate data of E_{k} is used. As per IEC standard [1] the E_{k} on the nameplate is the minimum value, which can be (even considerably) smaller than the real (measured) knee-point emf.

3.7 Final check of the scheme sensitivity

In the final stage the final scheme sensitivity can be chosen by applying the Eq. (21) with known varistor spill current, as per Eq.(16).

$$I_{\mathrm{p,des,final}} = k_{\mathrm{r}} \cdot I_{\mathrm{set}} + k_{\mathrm{r}} \cdot \left(\sum_{x=1}^{N_{\mathrm{CT}}} \frac{U_{\mathrm{set}}}{E_{\mathrm{k,x}}} I_{\mathrm{e,x}} + I_{\mathrm{var}}(U_{\mathrm{set}}) \right) \approx k_{\mathrm{r}} \cdot \left[I_{\mathrm{set}} + N_{\mathrm{CT}} \frac{U_{\mathrm{set}}}{E_{\mathrm{k}}} I_{\mathrm{e}} + I_{\mathrm{var}}(U_{\mathrm{set}}) \right] \quad (21)$$

4 Working Example

This chapter provides working example showing relevant calculations for a chosen application.

Exemplarily, a busbar protection application is taken.

4.1 Relevant data required

4.1.1 Relevant power system data

The relevant power system primary data in case of busbar protection in transmission systems are taken as follows:

- the maximum symmetrical short-circuit current for external (through) faults $I''_{\text{sc,max,ext}} = 63\,\text{kA}$
- the maximum symmetrical short-circuit current for internal faults $I''_{\text{sc,max,int}} = 63\,\text{kA}$

In case of a busbar, for both above quantities the maximum short-time symmetrical short-circuit withstand current of the switchgear $I''_{\text{sc,max,swg}}$ is considered. :

- the rating of the circuit breakers / busbar rating equals to $I_{\text{r,load}} = 4000\ \text{A}$
- the minimum symmetrical short-circuit current for internal faults is assumed at $I''_{\text{sc,min,int}} = 15\,\text{kA}$ for phase-to-phase-fault current (as in typical solidly earthed transmission system the single-pole fault current at the busbar is slightly higher or slightly lower than the three-pole)

4.1.2 Relevant current transformer data

The CTs used in the high impedance scheme are of equal ratios, low leakage type of IEC class PX.

- the number of CT that belong to the considered /designed differential protection zone $N_{\text{CT}} = 8$

IEC class PX[1] parameters are as follows :

- CT ratio: 4000A/1A; i.e. $k_{\text{r}} = \frac{I_{\text{pr}}}{I_{\text{sr}}} = \frac{4000\ \text{A}}{1\ \text{A}} = 4000$
- CT knee-point emf $E_{\text{k}} = 1000\ \text{V}$
- CT exciting current at the knee-point emf $I_{\text{e}} = 25\,\text{mA}$
- CT secondary winding resistance $R_{\text{CT}} = 5\,\Omega$

Furthermore:

- the CT secondary wiring resistance from the CT clamps to the paralleling point of the scheme (loop resistance) equals to $R_{\text{wire}} = 0.55\,\Omega$ (corresponds to approx. 100 m loop length of copper wire with 4 mm^2 cross-section, resistance value is corrected to 75 $^{\text{O}}$C e.g. for worst case calculation)

4.1.3 Relevant relay data and necessary auxiliary component elements

The multifunctional relay 7SJ6 will be used for phase-selective high impedance busbar protection application. Thereby three standard inputs Q1..Q6 will be used:

- operating current setting range $I_{\text{set,range}} = 0.1\ \text{A}...0.01..35\ \text{A}$,
- relay input burden, expressed as resistance $R_{\text{relay}} = 0.05\,\Omega$.
- the data of the system components (resistor and varistor) will be calculated in further steps

4.2 Calculation of the minimum required stabilizing voltage

As per Eq (1) the minimum required stability voltage of the high impedance scheme U_{stab} can be calculated, taking the given maximum through fault current $I''_{sc,max,ext} = 63\,kA$:

$$U_{stab} = \frac{I_{max,ext}}{k_r}\left(R_{CT} + R_{wire}\right) = \frac{63kA}{4000}(5 + 0.55) = 87.41\,V \tag{22}$$

The setting voltage U_{set} of the scheme over the differential branch shall be made equal or greater than the required stability voltage, as calculated in Eq.(22). Let's take:

$$U_{set} = 120\,V \tag{23}$$

4.3 Calculation of the required fault setting

To assure the functionality of the scheme (trip on internal fault), the CT knee-point emf E_k shall fulfill the requirement as given in Eq (3):

$$E_k \geq 2 \cdot U_{set}\text{ , i.e.: } 1000\,V \geq 2 \cdot 120\,V = 240\,V \Rightarrow \text{fulfilled} \tag{24}$$

In order to reach the desired scheme sensitivity, i.e. to trip on internal fault, the current setting of the relay in the differential branch shall be now calculated.

Considering that the minimum fault current at the busbar is quite high, the desired primary fault sensitivity $I_{p,des}$ is chosen (exemplarily for this working example) at 50 % of the rating of the busbar:.

$$I_{p,des} = 2000\,A \tag{25}$$

Remark: Please note that the primary fault sensitivity for busbar can be chosen at different level. This depends on customer philosophy and experience.

Having chosen the primary fault sensitivity $I_{p,des}$ of the scheme, the secondary setting of the relay I_{set} can be calculated as per Eq. (6). The varistor spill current will be at this stage neglected:

$$I_{set} \approx \frac{I_{p,des}}{k_r} - N_{CT}\frac{U_{set}}{E_k}I_e - I_{var}(U_{set}) = \frac{2000\,A}{4000} - 8\frac{120\,V}{1000\,V}0.025\,A = 0.476\,A \tag{26}$$

The setting current I_{set} of the scheme will be then taken:

$$I_{set} = 0.5\,A \tag{27}$$

4.4 Calculation of the required stabilizing resistor

With the scheme setting voltage U_{set} and the current setting of the relay I_{set} . the resistance value of the external stabilizing resistor R_{stab} can be calculated as per Eq.(7):

$$R_{stab} = \frac{U_{set}}{I_{set}} - R_{relay} \approx \frac{U_{set}}{I_{set}} = \frac{120\,V}{0.5\,A} = 240\,\Omega \tag{28}$$

Thereby, the relay input burden R_{relay} was neglected.

The thermal rating of the resistor is calculated:

The continuous power rating of the stabilizing resistor can be chosen as per Eq. (17):

$$P_{\text{stab,cont}} \geq \frac{U_{\text{set}}{}^2}{R_{\text{stab}}} = \frac{120^2\ \text{V}^2}{240\,\Omega} = 60\ \text{W} \tag{29}$$

Remark: It shall be noted that in order to keep the resistor healthy during commissioning tests the fault current from the testing equipment should be immediately withdrawn after the device gives a protection trip.

Furthermore, R_{stab} must have a short time rating large enough to withstand the fault current before the fault is cleared. Thereby, the rms voltage developed across the stabilizing resistor during maximal prospective internal fault $U_{\text{rms,f}}$ is decisive for the thermal stress of the stabilizing resistor. It is calculated according to Eq.(18):

$$U_{\text{rms,f}} = 1.3 \cdot \sqrt[4]{E_{\text{k}}{}^3 \cdot R_{\text{stab}} \cdot \frac{I_{\text{sc,max,int}}}{k_{\text{r}}}} = 1.3 \cdot \sqrt[4]{(1000\ \text{V})^3 \cdot 240\,\Omega \cdot \frac{63000\ \text{A}}{4000}} = 1812.7\ \text{V} \tag{30}$$

The time duration of 0.5 seconds can be typically considered for the stabilizing resistor ($P_{\text{stab,0.5s}}$).

The resulting short-time rating $P_{\text{stab,0.5s}}$ shall be then chosen as per Eq.(19) :

$$P_{\text{stab,0.5s}} \geq \frac{U_{\text{rms,f}}{}^2}{R_{\text{stab}}} = \frac{(1812.7\ \text{V})^2}{240\,\Omega} = 13691\ \text{W} \tag{31}$$

Therefore:

Resistor chosen (per relay input): $R_{\text{stab}} = 240\,\Omega$, $P_{\text{stab,cont}} \geq 60\text{W}$, $P_{\text{stab,0.5s}} \geq 13691\ \text{W}$ (32)

Regarding short-time thermal rating remarks in chapter 0 shall be considered in case when size of resistor shall be too large for the given protection cubicle.

4.5 Calculation for the required non-linear resistor (varistor)

During an internal fault high voltage may arise across the differential branch (i.e. the tie with relay and R_{stab} connected in series). Therefore, non-linear resistors are necessary in order to avoid secondary circuits (wirings, CT clamps, resistors, etc) be exposed to high voltages. Such varistors shall be connected across the differential branch.

In order to estimate this voltage which may appear in the designed scheme, at first the theoretical rms voltage $U_{\text{sc,max,int,rms}}$ which would occur across the differential branch if CT did not saturate is determined according to Eq.(8):

$$U_{\text{sc,max,int,rms}} = \frac{I''_{\text{sc,max,int}}}{k_{\text{r}}} \left(R_{\text{relay}} + R_{\text{stab}}\right) = \frac{63\,\text{kA}}{4000} (0.05\,\Omega + 240\,\Omega) = 3780\ \text{V} \tag{33}$$

Considering CT saturation, the resulting maximum peak voltage across the differential branch $\hat{U}_{\text{max,tie}}$ is calculated:

$$\hat{U}_{\text{max,tie}} = 2\sqrt{2E_{\text{k}}\left(U_{\text{sc,max,int,rms}} - E_{\text{k}}\right)} = 2\sqrt{2000\ \text{V}\left(3780\ \text{V} - 1000\ \text{V}\right)} = 4716\ \text{V} \tag{34}$$

When the relationship in (10) is fulfilled the usage of varistor is mandatory:

$$\hat{U}_{\text{max,tie}} > 2000\,\text{V} \Leftrightarrow 4716\,\text{V} > 2000\,\text{V} \Rightarrow \text{varistor necessary} \tag{35}$$

Considering scheme setting voltage U_{set} of 120 V (very close to the recommended limit of 125 V for the smaller varistor) a Varisor of type 600A/S3/1/S1195 (three pole) or three varistor of type 600A/S1/S1088 can be chosen (see Table 1).

The protection level of this varistor can be estimated from its characteristic (for dc or instantaneous values) where the constants C and β are given in Table 1 and the maximum prospective secondary current for the internal fault:

$$\hat{U}_{\text{var}} = C \cdot \hat{I}^{\ \beta} = 900 \cdot \left(\sqrt{2} \cdot \frac{63000}{4000} \right)^{0.25} = 1955\,\text{V}\,, \tag{36}$$

The rms protection level is then:

$$U_{\text{var}} \sim \hat{U}_{\text{var}} / \sqrt{2} = 1383\,\text{V}\,, \tag{37}$$

Its rms spill current at the setting voltage of the scheme (Eq.(16):

$$I_{\text{var}} = 0.52 \cdot \left(\sqrt{2} \cdot \frac{U_{\text{set}}}{C} \right)^{1/\beta} = 0.66\,\text{mA} \tag{38}$$

The requirement that at the setting voltage the spill current shall be less than 30 mA (CTs with 1 A secondary) is then fulfilled.
The necessary thermal rating of the varistor can be calculated using Eq.(13)

$$P_{\text{var}} = \frac{4}{\pi} \cdot \frac{I_{\text{sc,max,int}}}{k_{\text{r}}} E_{\text{k}} = \frac{4}{\pi} \cdot \frac{63000\,\text{A}}{4000} 1000\,\text{V} = 20053.5\,\text{J/s} \tag{39}$$

This necessary thermal rating is smaller than the maximum thermal rating of 88000 J (see Table 1).This maximum energy rating will not be even exceeded by the short-circuit flow of 4 s.
Therefore:

Varistor chosen: one of 600A/S3/1/S1195 (three pole) type
or three varistors of type 600A/S1/S1088 (40)

4.6 Final check of the scheme sensitivity

In the final stage the final scheme sensitivity can be chosen by applying the Eq. (21) with known varistor spill current, as per calculation in Eq.(38):

$$\begin{aligned} I_{\text{p,des,final}} &\approx k_{\text{r}} \cdot \left[I_{\text{set}} + N_{\text{CT}} \frac{U_{\text{set}}}{E_{\text{k}}} I_{\text{e}} + I_{\text{var}}(U_{\text{set}}) \right] = \\ &= 4000 \cdot \left[0.5\,\text{A} + 8 \frac{120\,\text{V}}{1000\,\text{V}} 0.025\,\text{A} + 0.00066\,\text{A}) \right] = 4000 \cdot 0.52466\,\text{A} = 2098.6\,\text{A} \end{aligned} \tag{41}$$

This corresponds to 52.4 % of the rating of the busbar (4000 A) and fulfills the requested fault setting for this example.

4.7 Scheme settings

The stage I>>in the multifunctional relay 7SJ6 is then set for the main function (high impedance protection trip) with the following settings:

1220A	I>> measurement of	Fundamental component	
1214A	I>> active	Always	
1202	I>> Pickup	0.5 A (=. I_{set})	Range: 0.1A ...35A, stps. 0.01A
1203	I>> Time Delay	0.0 sec (Trip)	Range: 0s ...60s, stps. 0.01s

Furthermore the following high impedance scheme components are necessary:

Resistor chosen (pro relay input):	$R_{stab} = 240\,\Omega$, $P_{stab,cont} \geq = 60$ W , $P_{stab,0.5s} \geq 13691$ W

Varistor chosen:	one of 600A/S3/1/S1195 (three pole) type or three varistors of type 600A/S1/S1088

4.7.1 CT supervision

The CT circuit supervision can be incorporated within the relay, as well. It can be realized using I> stage of the multifunctional relay 7SJ6:
Depending on the loading conditions, the CT supervision can be set to detect approx. 12 % of the full loading of the busbar, i.e. 0,12 · 4000 A = 480 A primary. The secondary setting that can be incorporated will be then 0.1 A (24 V setting of the scheme) correspondingly. This leads to the final supervision sensitivity as per Eq (42):

$$I_{superv} \approx k_r \cdot \left[I_{set} + N_{CT} \frac{U_{set}}{E_k} I_e + I_{var}(U_{set}) \right] = \\ = 4000 \cdot \left[0.1\,A + 8 \frac{120\,V}{1000\,V} 0.025\,A + 0.00066\,A) \right] = 4000 \cdot 0.12466\,A = 498.6\,A \quad (42)$$

This corresponds to 12.5 % of the rating of the busbar (4000 A) and fulfills the requested CT supervision setting for this example.

The corresponding settings of the I> stage will be:

1221A	I> measurement of	Fundamental component	
1204	I> Pickup	0.1 A (=. I_{superv})	Range: 0.1A ...35A, stps. 0.01A
1205	I> Time Delay	5.0 sec (or different)	Range: 0s ...60s, stps. 0.01s

It is important to configure the I> stage for issuing alarm only.
In general, there are several options for further use of the CT supervision alarm. In this worked example this alarm signal will be available after 5 sec based on the timer setting I> Time Delay. The following options can be chosen:

1. Sending the alarm only (via binary output or via communication protocol).
2. Additionally to 1, route the alarm signal within the relay in order to block the high set element I>> (Annunciation 1721 for blocking I>>).This will avoid a trip of the high impedance busbar protection in case of a through fault under CT broken wire conditions. Please note that this measure will not protect the CT inputs of the relay and the stabilizing resistor / varistor against damage under longer lasting through fault conditions.
3. Additionally to 1 and 2, energize an external CT shorting relay with one coil and at least four related contacts (e.g. 7PA23). The lock-out relay has to be energized by the CT supervision alarm signal. One contact

should be placed in front of the varistor to short circuit each CT input of 7SJ6. The fourth contact of the relay can be used for signaling the 'high impedance busbar out-of-service' information. The reset of the external lock-out relay has to be done manually.
This measure will protect the CT inputs of the relay and the stabilizing resistor against damage under longer lasting through fault conditions.

Alternatively (depending on customer practice), a separate CT supervision relay may be used.

The types of further auxiliary components like CT shortening relay, CB lock-out and test switches can be chosen as per respective customer practice.

4.8 Connection Example

A connection example for the working example is shown in Figure 2. Thereby CT supervision is realized with the relay (using I> stage).

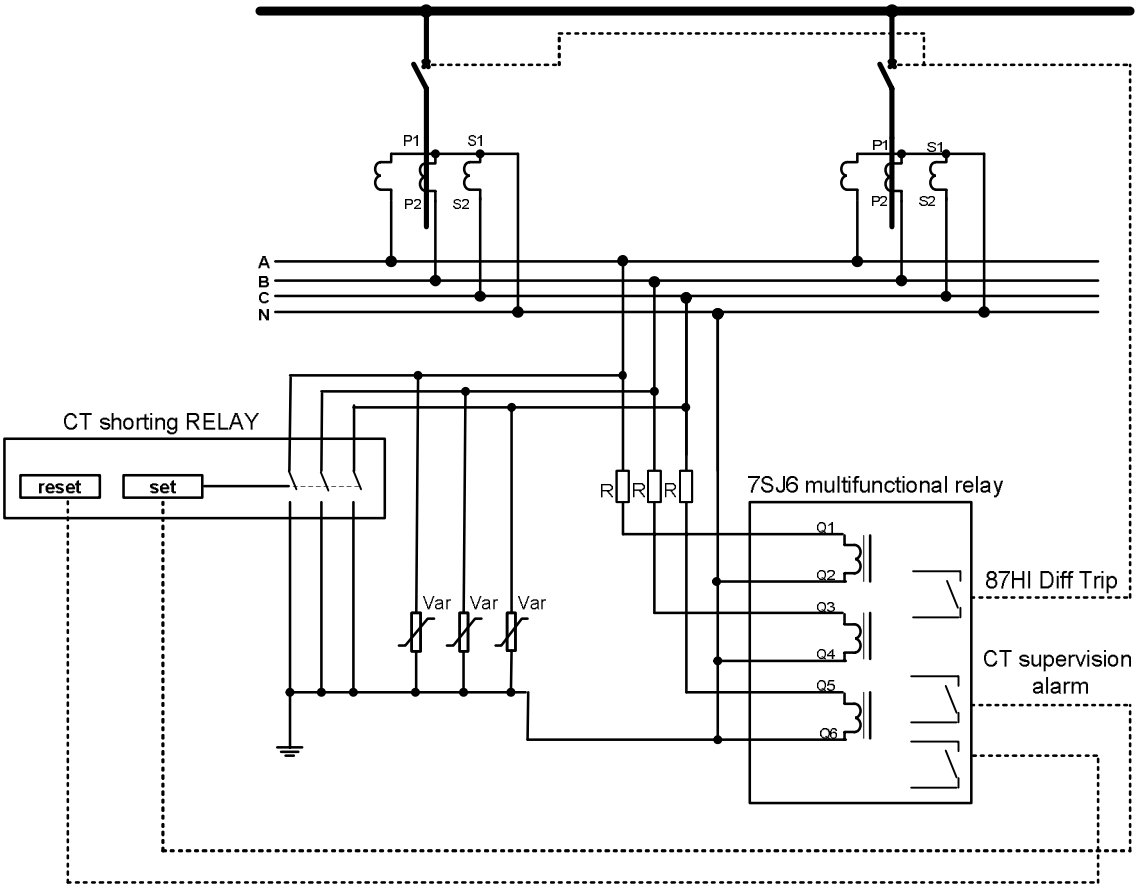

Figure 2 Connection of the high impedance scheme for the working example

5 Applications

As already mentioned in chapter 1 the multifunctional relay 7SJ6 can be used within all the mentioned high impedance protection schemes, both for phase-segregated circulating current high impedance protection applications, as well as for single phase restricted earth fault protection applications.

For the sake of completeness scheme setting hints for some major applications are shown in following.

5.1 Phase and earth-fault high impedance differential protection of busbars

The scheme stability setting (voltage over differential branch) [2]:

- maximum symmetrical short-circuit withstand current of the switchgear

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below:

- 10.. 30 % of minimum fault current available as per standard [2] , or as may be agreed
- %. of busbar rating (e.g. 33 % or 50 %)
- % of outgoing feeder rating (e.g. 100 % or 120 %)

Remark: High impedance protection scheme is widely used for busbar arrangements like single busbars, single busbars with sectionalizers, or circuit-breaker-and-a-half arrangements. The usage of high impedance busbar protection for double- and more sections busbars (with isolators) is not recommended, because of high complexity related to switching-over of CT secondaries that decreases the scheme reliability.

The high impedance protection scheme for busbar is shown exemplarily in Figure 3

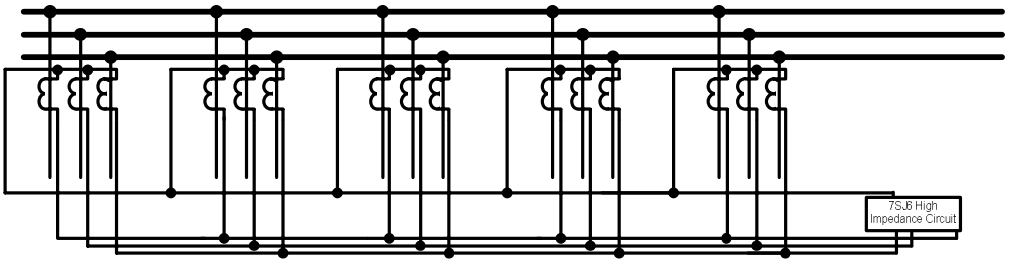

Figure 3 Phase and earth-fault high impedance differential protection of busbars

5.2 Phase and earth-fault high impedance differential protection of auto-transformers

The scheme stability setting (voltage over differential branch):

- maximum symmetrical short-circuit current for external faults (through-faults) at the LV side of the transformer, the latter can be taken as of 16 times the rated current of the LV side of the transformer (or other value as may be agreed) as per [2]

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below [2]:

- for transformer winding solidly connected to earth: 10.. 60 % of the rated current of the HV winding
- for transformers winding earthed via impedance 10.. 25 % of minimum fault current available for an earth-fault at transformer terminals

The high impedance protection scheme for auto-transformers is shown exemplarily in Figure 4

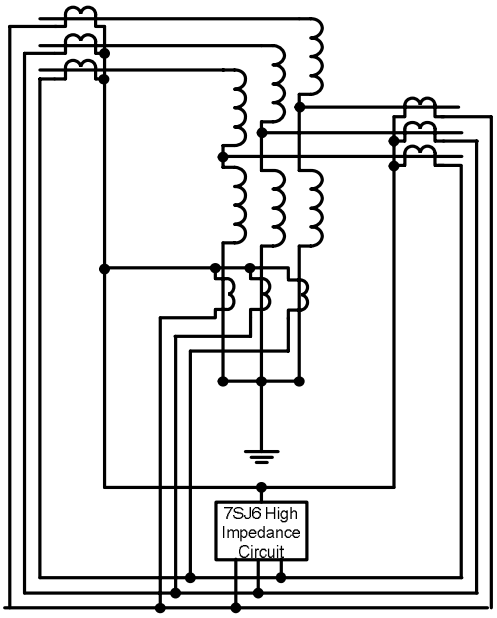

Figure 4 Phase and earth-fault high impedance differential protection of auto-transformers

5.3 Phase and earth-fault high impedance differential protection of motors or generators (synchronous)

The scheme stability setting (voltage over differential branch):

- maximum symmetrical short-circuit current for external faults (through-faults) of the synchronous machines, the latter can be taken as of 12.5 times the rated current of the series reactor winding (or other value as may be agreed) as per [2]

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below [2]:

- less than 10 % of the rated current of the proteted winding of the synchronous machine

5.4 Phase and earth-fault high impedance differential protection of series reactors

The scheme stability setting (voltage over differential branch):

- maximum symmetrical short-circuit current for external faults (through-faults) of the series reactor, the latter can be taken as of 20 times the rated current of the series reactor winding (or other value as may be agreed) as per [2]

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below [2]:

- 10.. 30 % of minimum fault current available for a-fault at series reactor terminals

5.5 Phase and earth-fault high impedance differential protection of shunt reactors

The scheme stability setting (voltage over differential branch):

- maximum symmetrical short-circuit current for external faults (through-faults) of the shunt reactor, the latter can be taken as of 10 times the rated current of the shunt reactor winding (or other value as may be agreed) as per [2]

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below [2]:

- 10.. 25 % of minimum fault current available for a-fault at shunt reactor terminals

In Figure 5 high impedance scheme of series reactors, shunt reactors, motors or generators is shown

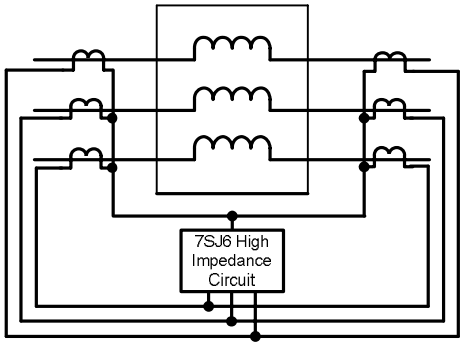

Figure 5 Phase and earth-fault high impedance differential protection of series reactors, shunt reactors, motors or generators

5.6 Restricted earth fault (REF) protection schemes of transformer windings

The scheme stability setting (voltage over differential branch):

- maximum symmetrical short-circuit current for external faults (through-faults) of the protected transformer winding, the latter can be taken as of 16 times the rated current of the protected winding of the transformer (or other value as may be agreed) as per [2]

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below [2]:

- for transformer winding solidly connected to earth: 10.. 60 % of the rated current of the winding
- for transformers winding earthed via impedance or isolated: 10.. 25 % of minimum fault current available for an earth-fault at transformer terminals

The high impedance protection scheme for transformer windings is shown exemplarily in Figure 6.

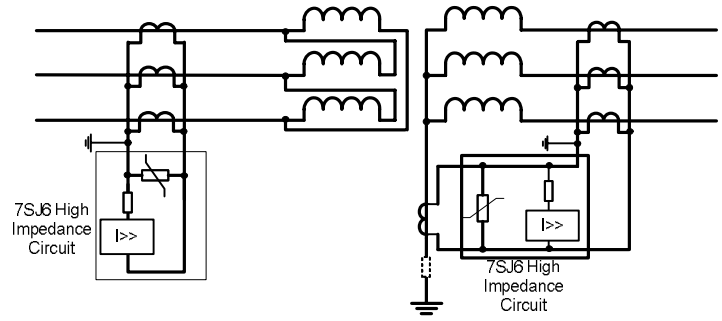

Figure 6 Restricted earth-fault high impedance differential protection of transformers

6 References

[1] International Standard IEC 61869-2, Edition 1.0, 2012-09, Instrument Transformers – Part.2: Additional requirements for current transformers

[2] ENA Energy Network association: Technical Specification 48-3, Issue 2 2013, Instantaneous high-impedance differential protection

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